AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amendedl) A method for providing a horizontal scan control signal for a TV set from a horizontal synchronization signal contained in a composite video signal, the horizontal synchronization signal containing horizontal synchronization pulses and parasitic pulses, said scan control signal being provided from an oscillating signal generated by an oscillator of a phase-locked loop receiving the horizontal synchronization signal, said oscillating signal having a frequency depending on a driving signal provided from the comparison between the horizontal synchronization signal and a binary phase signal, wherein, at each parasitic pulse among successive parasitic pulses between two synchronization pulses, the driving signal is ~~successively~~ alternately varied in the increasing direction [[or]] and in the decreasing direction.

2. (Original) The method of claim 1, wherein the parasitic pulses have variable durations.

3. (Currently amended) A circuit for providing a horizontal scan control signal for a TV set from a horizontal synchronization signal contained in the composite video signal, the horizontal synchronization signal containing horizontal synchronization pulses and parasitic pulses, said circuit comprising a phase-locked loop receiving the horizontal synchronization signal comprising an oscillator generating an oscillating signal from which is provided the scan control signal, the frequency of the oscillating [[circuit]] signal depending on a driving signal provided from the horizontal synchronization signal, and comprising a means for correcting the driving signal which, at each parasitic pulse among successive parasitic pulses between two synchronization pulses, alternately varies the driving signal in the increasing [[or]] and decreasing direction.

4. (Currently amended) The [[method]] circuit of claim 3, further comprising:

a comparator for comparing the horizontal synchronization signal and a modified phase signal and providing, according to the comparison, a current of zero amplitude or of constant amplitude and of variable sign;

a capacitor conducting the current and providing the driving signal; and

a correction circuit providing the comparator with the modified phase signal corresponding to a binary phase signal having a frequency proportional to the frequency of the oscillating signal or corresponding to a binary correction signal, the state of which switches for each parasitic pulse.

5. (Original) The circuit of claim 4, wherein the correction circuit comprises a switch adapted to alternately connecting, according to a switch control signal, an output terminal connected to the comparator at a first input terminal receiving the phase signal or at a second input terminal receiving the correction signal, the switch signal being provided from a binary signal at a first state at the level of a synchronization pulse and at a second state otherwise.

6. (Original) The circuit of claim 5, wherein the switch signal is also provided from at least one binary validation signal at a first state when a validation condition is fulfilled and at a second state when the validation condition is not fulfilled.

7. (Original) The circuit of claim 4, comprising a latch providing the correction signal receiving a binary latch control signal provided from the horizontal synchronization signal, the state of the correction signal switching at each falling edge of the latch control signal.

8. (Original) The circuit of claim 7, comprising a filter receiving the horizontal synchronization signal and providing the latch control signal, the latch control signal comprising pulses, each pulse being associated with a parasitic pulse.

9. (New) A method of synchronizing an image signal with a synchronization signal that includes synchronization pulses, the method comprising:

receiving the synchronization signal;

providing a control signal to a phase-locked loop based on the synchronization signal;

determining a presence of parasitic pulses in the synchronization signal; and

in response to determining the presence of the parasitic pulses, adjusting the control signal such that an average of the control signal is approximately zero.

10. (New) The method of claim 9, wherein the adjusting of the control signal comprises adjusting the control signal such that the control signal has a pulse of alternating polarity for each one of the parasitic pulses received.

11. (New) The method of claim 9, wherein the providing of the control signal to the phase-locked loop based on the synchronization signal comprises:

comparing a phase-locked loop signal to the synchronization signal.

12. (New) The method of claim 11, wherein the adjusting of the control signal comprises comparing the synchronization signal to a signal that changes polarity in response to each parasitic pulse received.

13. (New) The method of claim 9, wherein the adjusting of the control signal comprises de-coupling the control signal from the phase-locked loop signal.

14. (New) A circuit for synchronizing an image signal with a synchronization signal that includes synchronization pulses, the circuit comprising:

a phase-locked loop that receives a control signal; and

a correction circuit that adjusts the control signal to have an average value of approximately zero, in response to determining a presence of parasitic pulses in the synchronization signal.

15. (New) The circuit of claim 14, further comprising:

a comparator that compares the synchronization signal with at least one other signal and provides the control signal to the phase-locked loop.

16. (New) The circuit of claim 15, wherein the at least one other signal comprises a phase-locked loop signal.

17. (New) The circuit of claim 15, wherein the at least one other signal comprises a signal that changes polarity in response to each parasitic pulse received.

18. (New) The circuit of claim 17, wherein the correction circuit comprises:

a switch that couples the comparator, in response to determining a presence of the parasitic pulses, to the signal that changes polarity.

19. (New) The circuit of claim 18, wherein the correction circuit further comprises:

a filter that receives the synchronization signal and removes the synchronization pulses therefrom, such that the filter provides a signal that includes only the parasitic pulses; and

a flip-flop that receives the signal that includes only the parasitic pulses, and provides to the comparator the signal that changes polarity.

20. (New) The circuit of claim 19, wherein the circuit provides a horizontal scan control signal for a TV set and the phase-locked loop comprises an oscillator that produces a signal having a frequency that is based on a magnitude of the control signal.